BUK754R0-55B; BUK764R0-55B

N-channel TrenchMOS standard level FET

Rev. 04 — 4 October 2007

Product data sheet

1. Product profile

1.1 General description

N-channel enhancement mode power Field-Effect Transistor (FET) in a plastic package using NXP High-Performance Automotive (HPA) TrenchMOS technology.

1.2 Features

- Very low on-state resistance
- 175 °C rated

- Q101 compliant
- Standard level compatible

1.3 Applications

- Automotive systems
- Motors, lamps and solenoids
- General purpose power switching
- 12 V and 24 V loads

1.4 Quick reference data

- \blacksquare E_{DS(AL)S} \leq 1.2 J
- $I_D \le 75 A$

- \blacksquare R_{DSon} = 3.4 mΩ (typ)
- Arr P_{tot} \leq 300 W

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline		Symbol	
1	gate (G)			_	
2	drain (D)	mb C	mb	D	
3	source (S)				
mb	mounting base; connected to drain (D)	1 2 3 03ab54	mbb076 S SOT404 (D2PAK)		
		SOT78A (TO-220AB))		



3. Ordering information

Table 2. Ordering information

Type number	Package					
	Name	Description	Version			
BUK754R0-55B	SC-46	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78A			
BUK764R0-55B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404			

4. Limiting values

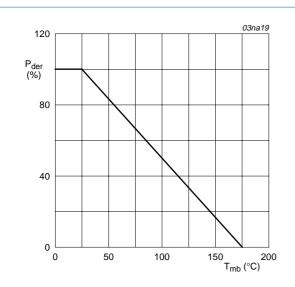
Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage			-	55	V
V_{DGR}	drain-gate voltage (DC)	$R_{GS} = 20 \text{ k}\Omega$		-	55	V
V_{GS}	gate-source voltage			-	±20	V
I _D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V;	[1][3]	-	193	Α
		see Figure 2 and 3	[2]	-	75	Α
		$T_{mb} = 100 ^{\circ}C; V_{GS} = 10 V; see \underline{Figure 2}$	[2]	-	75	Α
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \mu s$; see Figure 3		-	774	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; see <u>Figure 1</u>		-	300	W
T _{stg}	storage temperature			-55	+175	°C
Tj	junction temperature			-55	+175	°C
Source-d	Irain diode					
I _{DR}	reverse drain current	T _{mb} = 25 °C	[1][2]	-	193	Α
			[2]	-	75	Α
I _{DRM}	peak reverse drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \mu s$		-	774	Α
Avalanch	ne ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	unclamped inductive load; I_D = 75 A; $V_{DS} \le$ 55 V; R_{GS} = 50 Ω ; V_{GS} = 10 V; starting at T_j = 25 °C		-	1.2	J
E _{DS(AL)R}	repetitive drain-source avalanche energy		<u>[4]</u>	-	-	J

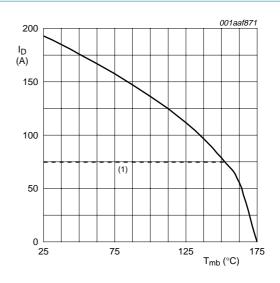
- [1] Current is limited by chip power dissipation rating.
- [2] Continuous current is limited by package.
- [3] Refer to document 9397 750 12572 for further information.
- [4] Conditions:
 - a) Maximum value not quoted. Repetitive rating defined in Figure 16.
 - b) Single-pulse avalanche rating limited by T_{j(max)} of 175 °C.
 - c) Repetitive avalanche rating limited by an average junction temperature of 170 $^{\circ}\text{C}.$
 - d) Refer to application note AN10273 for further information.

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$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

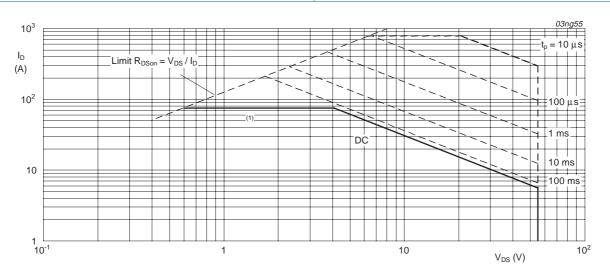
Fig 1. Normalized total power dissipation as a function of mounting base temperature



 $V_{GS} \ge 10 \text{ V}$

(1) Capped at 75 A due to package.

Fig 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is single pulse

(1) Capped at 75 A due to package.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit	
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base		-	-	0.5	K/W	
R _{th(j-a)}	thermal resistance from junction to ambient						
	SOT78A (TO-220AB)	vertical in free air	-	60	-	K/W	
	SOT404 (D2PAK)	mounted on a printed-circuit board; minimum footprint	-	50	-	K/W	

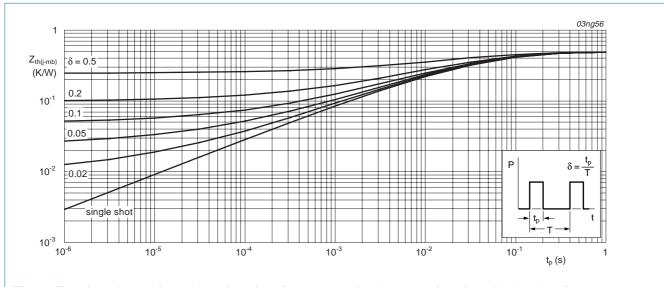


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

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6. Characteristics

Table 5. Characteristics

 $T_i = 25 \,^{\circ}C$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static ch	aracteristics					
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 V$				
		T _j = 25 °C	55	-	-	V
		T _j = −55 °C	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS} = V_{GS}$; see Figure 9				
		T _j = 25 °C	2	3	4	V
		T _j = 175 °C	1	-	-	V
		T _j = −55 °C	-	-	4.4	V
I _{DSS}	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}$				
		T _j = 25 °C	-	0.02	1	μΑ
		T _j = 175 °C	-	-	500	μΑ
I _{GSS}	gate leakage current	$V_{GS} = \pm 20 \text{ V}; V_{DS} = 0 \text{ V}$	-	2	100	nA
R _{DSon} drain-source on-state resistance	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A};$ see Figure 6 and 8	2.4			
		T _j = 25 °C	-	3.4	4.0	$m\Omega$
		T _j = 175 °C	-	-	8	$m\Omega$
Dynamic	characteristics					
Q _{G(tot)}	total gate charge	$I_D = 25 \text{ A}; V_{DD} = 44 \text{ V}; V_{GS} = 10 \text{ V};$		86	-	nC
Q _{GS}	gate-source charge	see Figure 14	-	18	-	nC
Q_{GD}	gate-drain charge			25	-	nC
C _{iss}	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	5082	6776	pF
Coss	output capacitance	see Figure 12		1054	1265	pF
C _{rss}	reverse transfer capacitance		-	450	617	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \Omega;$	-	23	-	ns
t _r	rise time	V_{GS} = 10 V; R_G = 10 Ω	-	51	-	ns
t _{d(off)}	turn-off delay time		-	71	-	ns
t _f	fall time		-	41	-	ns
L _D	internal drain inductance	from drain lead 6 mm from package to center of die	-	4.5	-	nΗ
		from contact screw on mounting base to center of die SOT78A	-	3.5	-	nΗ
		from upper edge of drain mounting base to center of die SOT404	-	2.5	-	nΗ
L _S	internal source inductance	from source lead to source bonding pad	-	7.5	-	nΗ
Source-d	rain diode					
V_{SD}	source-drain voltage	$I_S = 40 \text{ A}; V_{GS} = 0 \text{ V}; \text{ see } \frac{\text{Figure 15}}{\text{Figure 15}}$	-	0.85	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s};$	-	95	-	ns
Qr	recovered charge	$V_{GS} = -10 \text{ V}; V_R = 30 \text{ V}$	-	251	-	nC

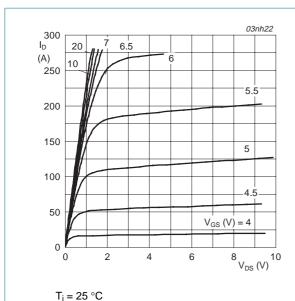


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

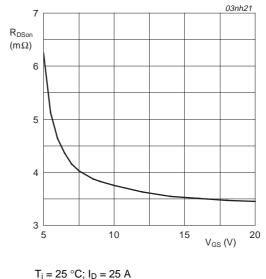


Fig 6. Drain-source on-state resistance as a function

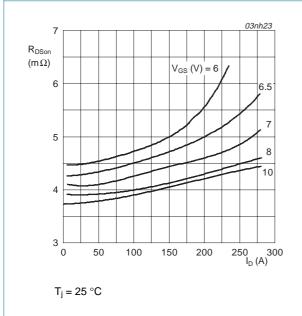
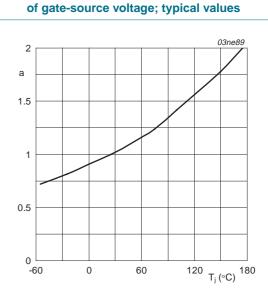


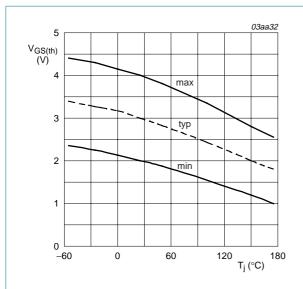
Fig 7. Drain-source on-state resistance as a function of drain current; typical values



 $a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$

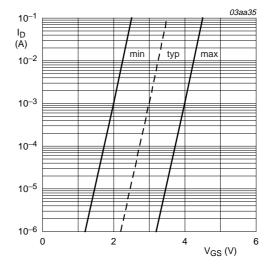
Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature

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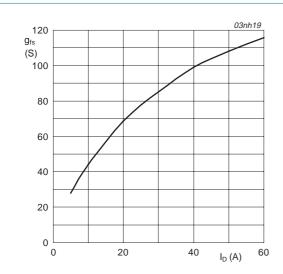
 $I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



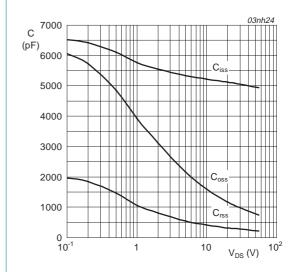
 $T_i = 25 \,^{\circ}C; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



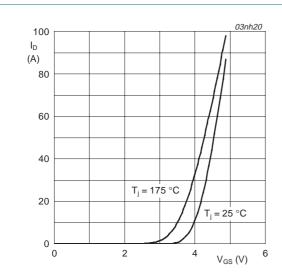
 $T_i = 25 \,^{\circ}C; \, V_{DS} = 25 \,^{\circ}V$

Fig 11. Forward transconductance as a function of drain current; typical values



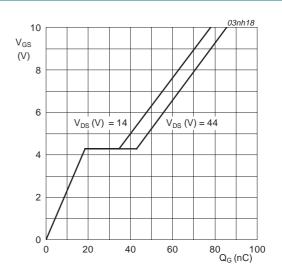
 $V_{GS} = 0 V; f = 1 MHz$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



 $V_{DS} = 25 \text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values



 $T_i = 25 \,^{\circ}C; I_D = 25 \,^{\circ}A$

Fig 14. Gate-source voltage as a function of gate charge; typical values

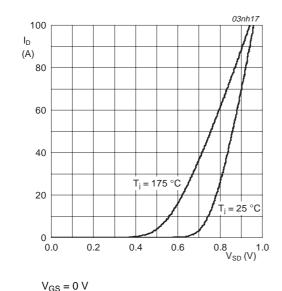
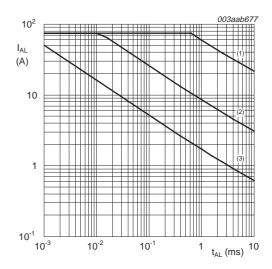


Fig 15. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



See Table note 4 of Table 3 Limiting values.

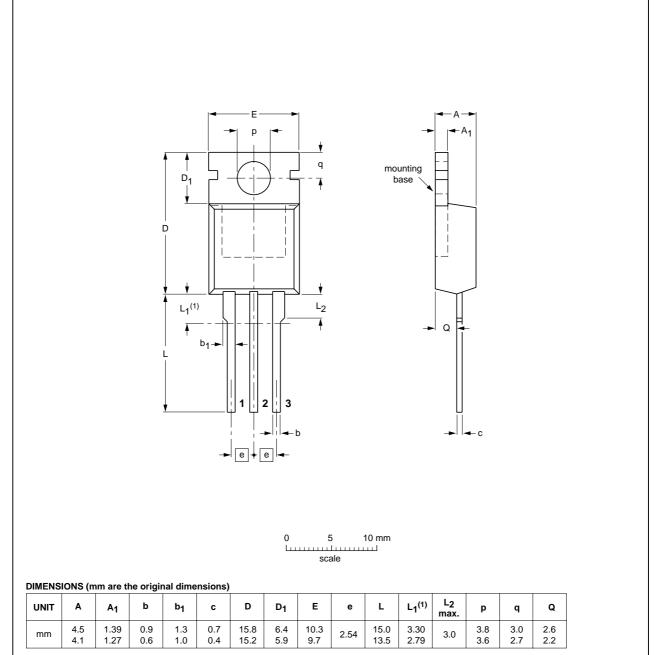
- (1) Single-pulse; T_i = 25 °C.
- (2) Single-pulse; T_i = 150 °C.
- (3) Repetitive.

Fig 16. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78A



Note

1. Terminals in this zone are not tinned.

OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA	PROJECTION	1990E DATE	
SOT78A		3-lead TO-220AB	SC-46		03-01-22 05-03-14	

Fig 17. Package outline SOT78A (TO-220AB)

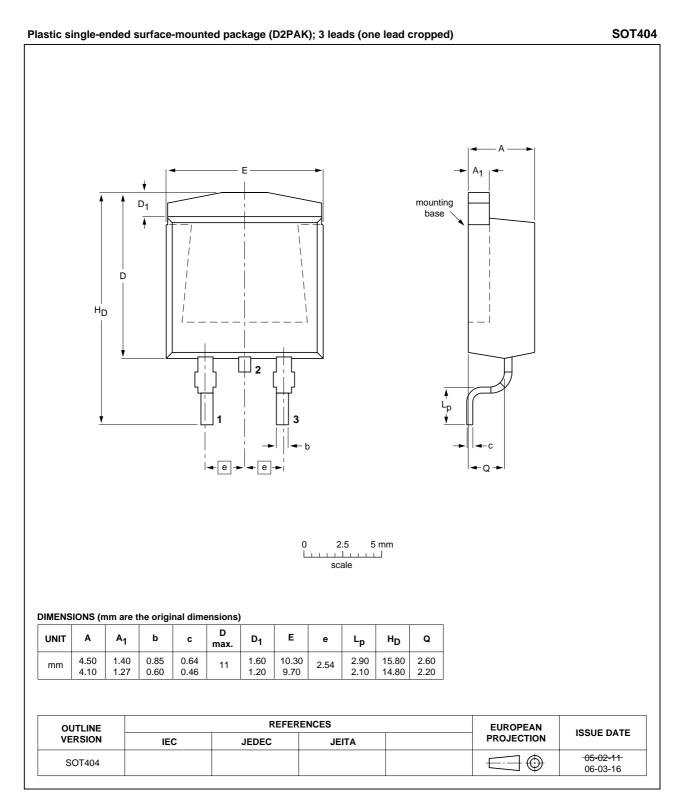
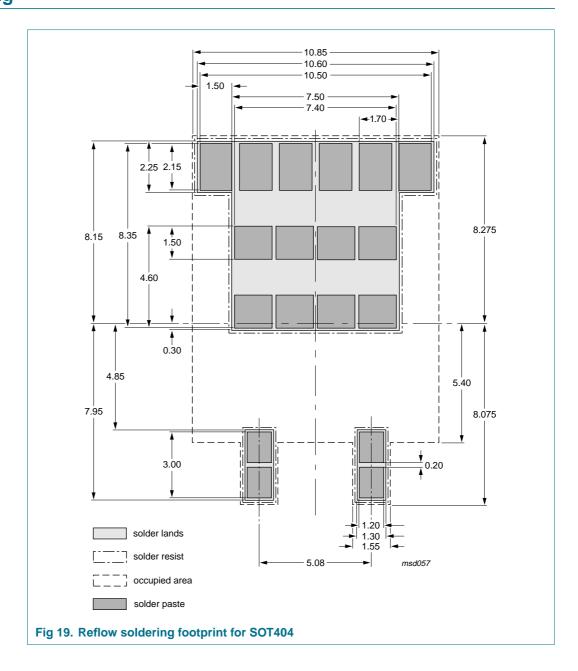


Fig 18. Package outline SOT404 (D2PAK)

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8. Soldering



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9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK75_764R0-55B_4	20071004	Product data sheet	-	BUK75_764R0-55B_3
Modifications:	 Figure 7 updated. 			
BUK75_764R0-55B_3	20070124	Product data sheet	-	BUK75_764R0_55B-02
 Modifications: The format of this data sheet has been redesigned to comply with the new identity g of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. 				appropriate.
	 C_{rss} (typ) and (max (max) to 450 (typ) 	x) value in Section 6 "Cha and 617 (max).	aracteristics" changed f	rom 289 (typ) and 396
BUK75_764R0_55B-02	20020930	Product data sheet	-	BUK75_764R0_55B-01
BUK75 764R0 55B-01	20020328	Product data sheet	-	-

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10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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